

150V N-Channel Enhancement Mode MOSFET

1.Product Information

1.1 Features

- ◇ Advanced SGT cell design
- ◇ Low Gate Charge
- ◇ Low On-Resistance
- ◇ RoHS and Halogen-Free Compliant
- ◇ 100% ΔV_{DS} & UIS & Rg Tested

1.2 Applications

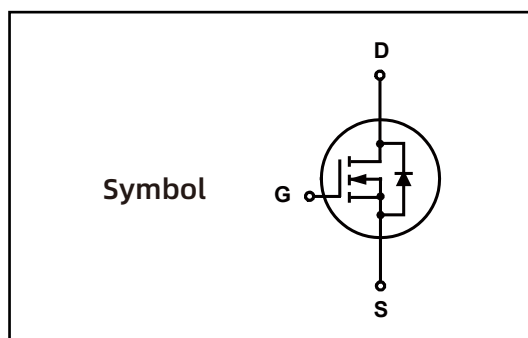
- ◇ DC-DC Converter
- ◇ Drones
- ◇ Motor drivers
- ◇ Light electric vehicles

1.3 Quick reference

- ◇ $BV \geq 150\text{ V}$
- ◇ $P_{\text{tot}} \leq 107\text{ W}$
- ◇ $I_D \leq 35\text{ A}$
- ◇ $R_{DS(ON)} \leq 52.0\text{ m}\Omega @ V_{GS} = 10\text{ V}$
- ◇ $R_{DS(ON)} \leq 58.0\text{ m}\Omega @ V_{GS} = 6.0\text{ V}$



2.Pin Description



Simplified Outline

Top View
PDFN3.3*3.3



3.Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit	Note
V_{DS}	Drain-Source Voltage	$T_C = 25\text{ }^{\circ}\text{C}$	-	150	V	-
V_{GS}	Gate-Source Voltage	$T_C = 25\text{ }^{\circ}\text{C}$	-	± 20	V	-
I_D^*	Drain Current (DC)	$T_C = 25\text{ }^{\circ}\text{C}, V_{GS} = 10\text{ V}$	-	35	A	Fig.2
		$T_C = 100\text{ }^{\circ}\text{C}, V_{GS} = 10\text{ V}$	-	22	A	
$I_{DM}^{**},^{***}$	Drain Current (Pulsed)	$T_C = 25\text{ }^{\circ}\text{C}, V_{GS} = 10\text{ V}$	-	57	A	-
P_{tot}	Drain power dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	-	107	W	Fig.1
		$T_C = 100\text{ }^{\circ}\text{C}$	-	43	W	
	Linear reduction	$T_A > 25\text{ }^{\circ}\text{C}$	-	0.85	W/ $^{\circ}\text{C}$	
T_{stg}	Storage Temperature		-55	150	$^{\circ}\text{C}$	-
T_J	Junction Temperature		-	150	$^{\circ}\text{C}$	-
I_S	Continuous-Source Current	$T_C = 25\text{ }^{\circ}\text{C}$	-	35	A	-
E_{AS}^*	Single Pulsed Avalanche Energy	$V_{DD} = 150\text{ V}, L = 0.1\text{ mH}$	-	63	mJ	Fig.19

4.Thermal Characteristics

$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient	-	34	$^{\circ}\text{C/W}$	Fig.16
$R_{\theta JC}^*$	Thermal Resistance- Junction to Case	-	1.16		

Notes :

- * Surface Mounted on 1 in² pad area, $t \leq 10\text{ sec}$
- ** Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- *** limited by bonding wire

5.Marking Information

Product Name	Package	Reel size	Tape width	Quantity	Note
LN490N150Q	PDFN3.3*3.3	330mm	12mm	5000	

Note: COMTECH defines “ Green ” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

6. Electrical Characteristics ($T_A=25^\circ$ Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
Static Characteristics							
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _{DS} = 250 μA	150	-	-	V	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	2	-	4	V	
I _{DSS}	Drain Leakage Current	V _{DS} =150V, V _{GS} = 0 V	-	-	1	μA	
I _{GSS}	Gate Leakage Current	V _{GS} = ± 20 V, V _{DS} = 0 V	-	-	±100	nA	
R _{DS(ON)} ^a	On-State Resistance	V _{GS} =10V , I _{DS} =5A	-	40.0	52.0	mΩ	Fig.8
		V _{GS} =6.0V, I _{DS} =5A	-	45.0	58.0		
Diode Characteristics							
V _{SD} ^a	Diode Forward Voltage	I _{SD} = 5A , V _{GS} = 0 V	-	-	1.3	V	Fig.7
t _{rr}	Reverse Recovery Time	I _{DS} = 5A , V _{GS} = 0 V dI _{SD} /dt = 100 A/μs	-	102	-	nS	Fig.20
Q _{rr}	Reverse Recovery Charge		-	121	-	nC	
Dynamic Characteristics ^b							
C _{ISS}	Input Capacitance	V _{GS} = 0 V, V _{DS} =75V Frequency = 1 MHz	-	1165	-	pF	Fig.10
C _{OSS}	Output Capacitance		-	86	-		
C _{rSS}	Reverse Transfer Capacitance		-	9	-		
R _G	Gate Resistance	F= 1 MHz	-	0.8	-	Ω	
t _{d(on)}	Turn-on Delay Time	V _{DS} =75V , V _{GS} = 10 V, R _G = 13.0Ω, R _L = 100uH I _{DS} = 5A	-	19	-	nS	Fig.18
t _r	Turn-on Rise Time		-	37	-		
t _{d(off)}	Turn-off Delay Time		-	48	-		
t _f	Turn-off Fall Time		-	24	-		
dv/dt(on)	Turn-on Peak Diode Recovery		-	1.603	-	KV/us	
dv/dt(off)	Turn-off Peak Diode Recovery		-	2.477	-		
di/dt(on)	Turn-on Peak Diode Recovery		-	355	-	A/us	
di/dt(off)	Turn-off Peak Diode Recovery		-	158	-		
Gate Charge Characteristics ^b							
Q _g	Total Gate Charge	V _{DS} =75V , V _{GS} = 10 V, I _{DS} = 5A	-	23	-	nC	Fig.9
Q _{gs}	Gate-Source Charge		-	4	-		
Q _{gd}	Gate-Drain Charge		-	5	-		
V _{plateau}	Gate plateau voltage		-	4.1	-	V	

Notes :

a : Pulse test ; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b : Guaranteed by design, not subject to production testing

7. Typical Characteristics

Fig.1 Power Capability

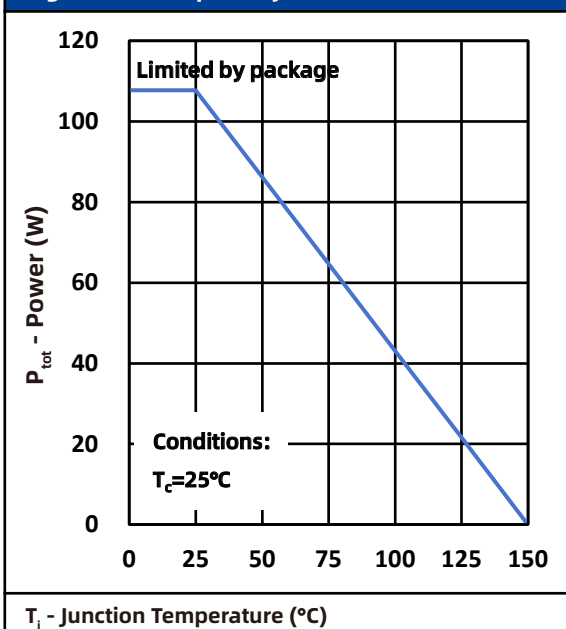


Fig.2 Current Capability

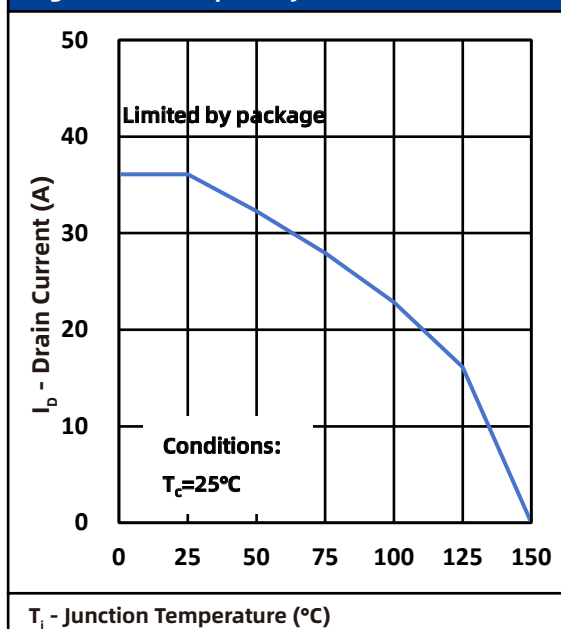


Fig.3 Output Characteristics@T_j -55°C

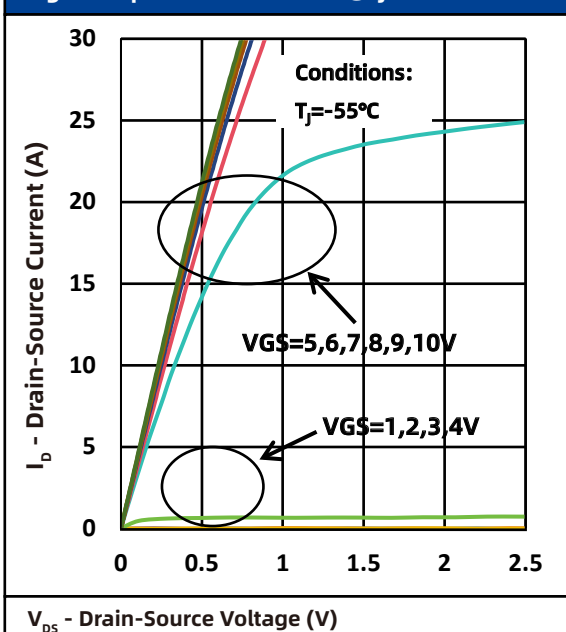
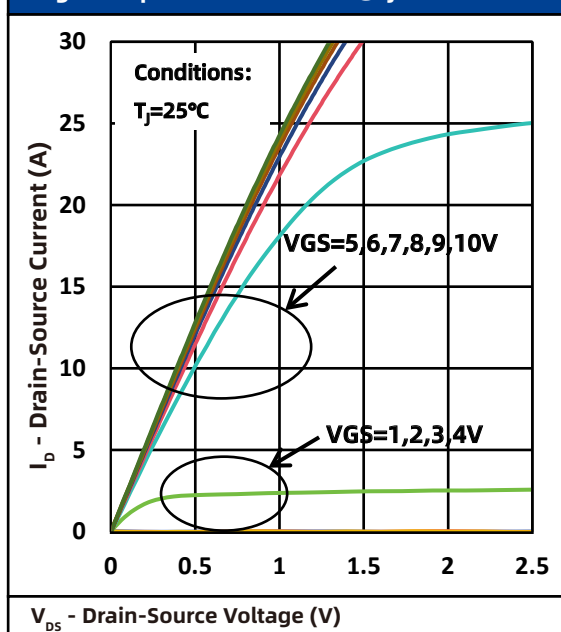


Fig.4 Output Characteristics@T_j 25°C



7. Typical Characteristics

Fig.5 Output Characteristics@Tj 150°C

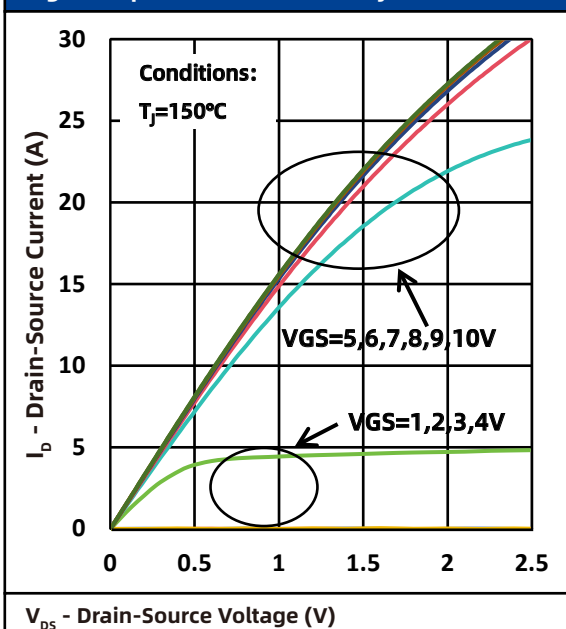


Fig.6 Transfer Characteristics vs Temp

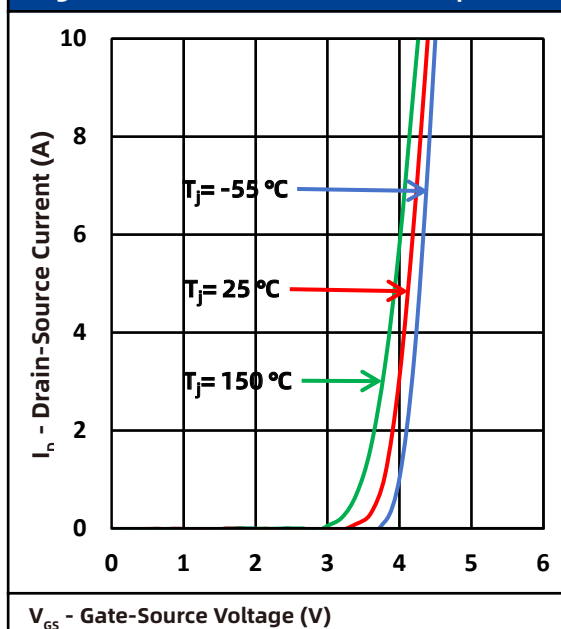


Fig.7 Body Diode Characteristics

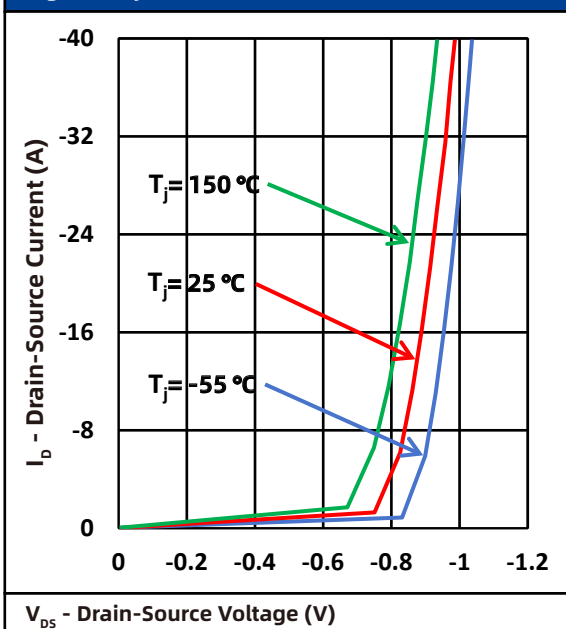
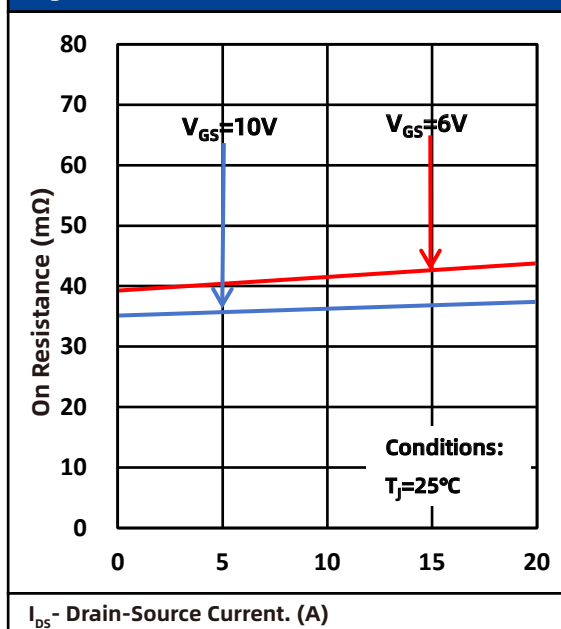


Fig.8 Drain-Source On Resistance



7. Typical Characteristics

Fig.9 Gate Charge

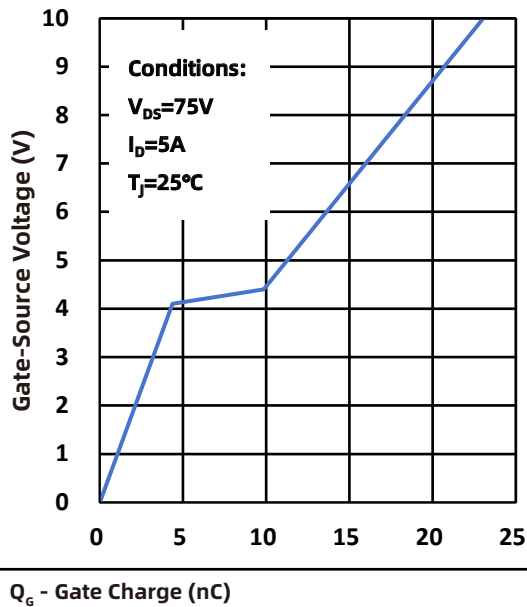


Fig.10 Capacitance

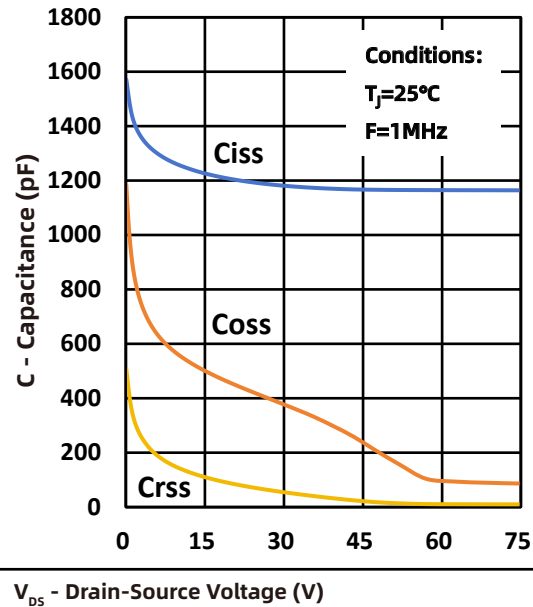


Fig.11 Normalized Threshold Voltage

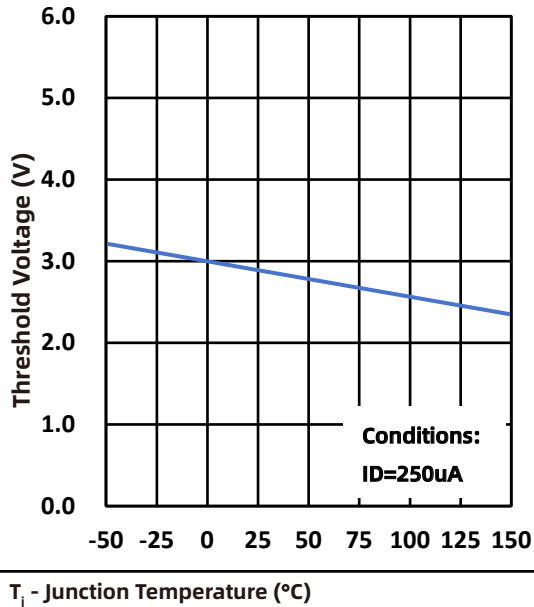
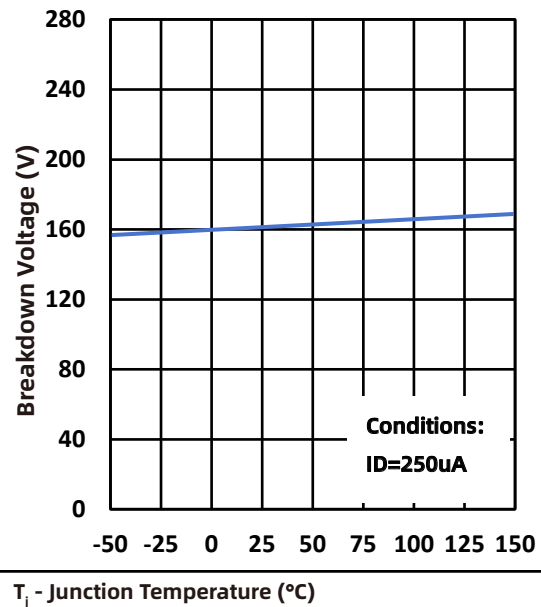


Fig.12 Normalized Breakdown Voltage



7. Typical Characteristics

Fig.13 Normalized On Resistance

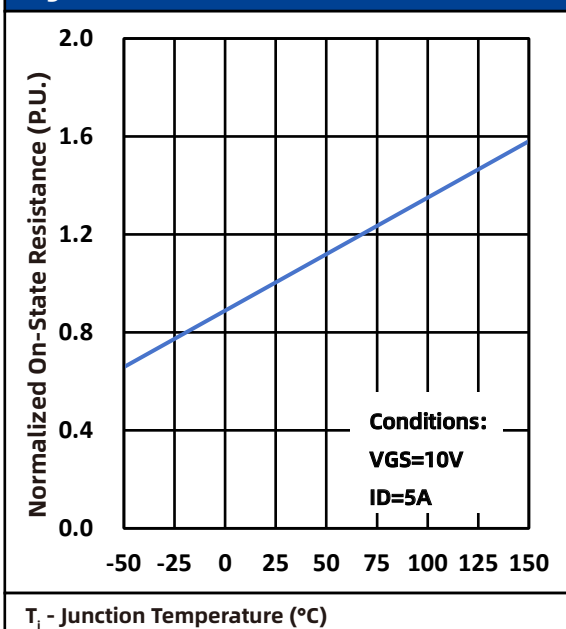


Fig.14 Switching Energy vs ID

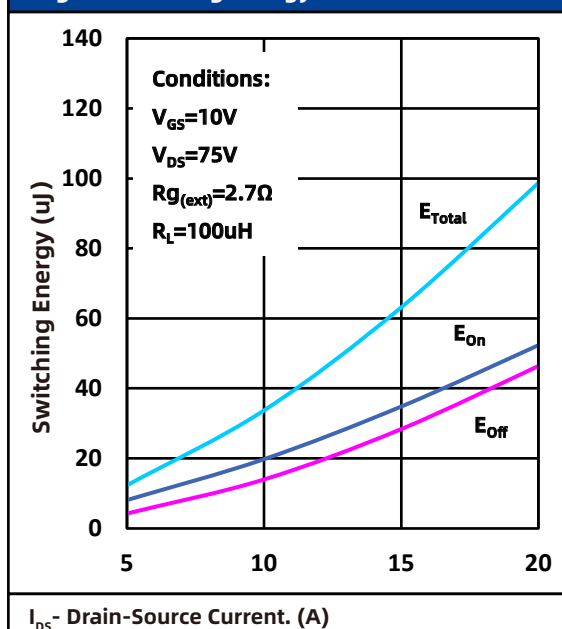


Fig.15 Safe Operating Area

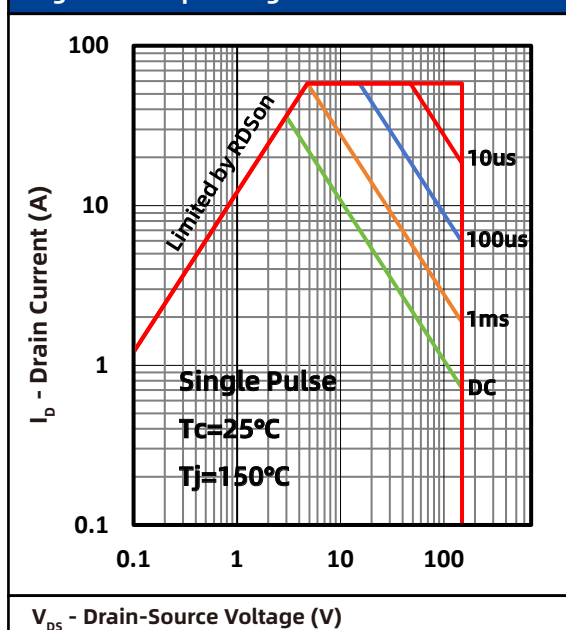


Fig.16 Transient Thermal Impedance

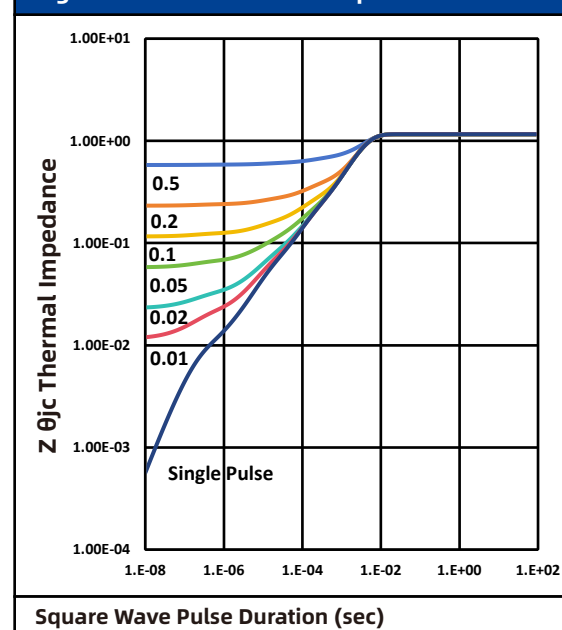
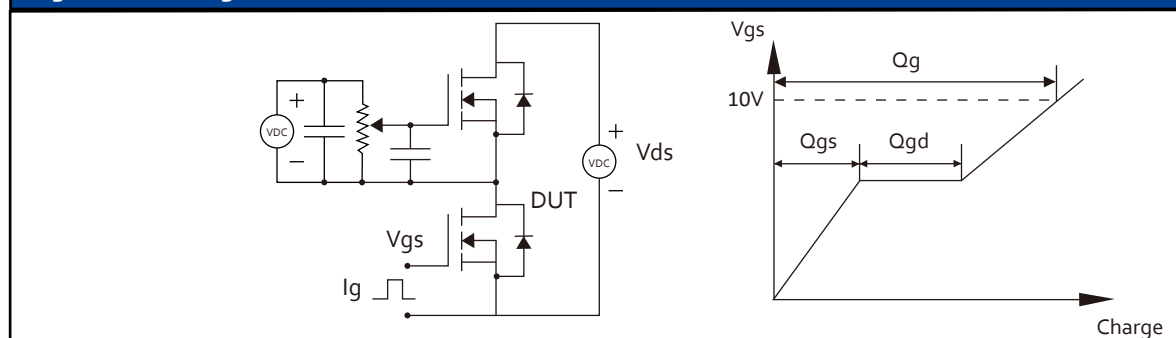


Fig.17 Gate Charge Test Circuit & Waveform



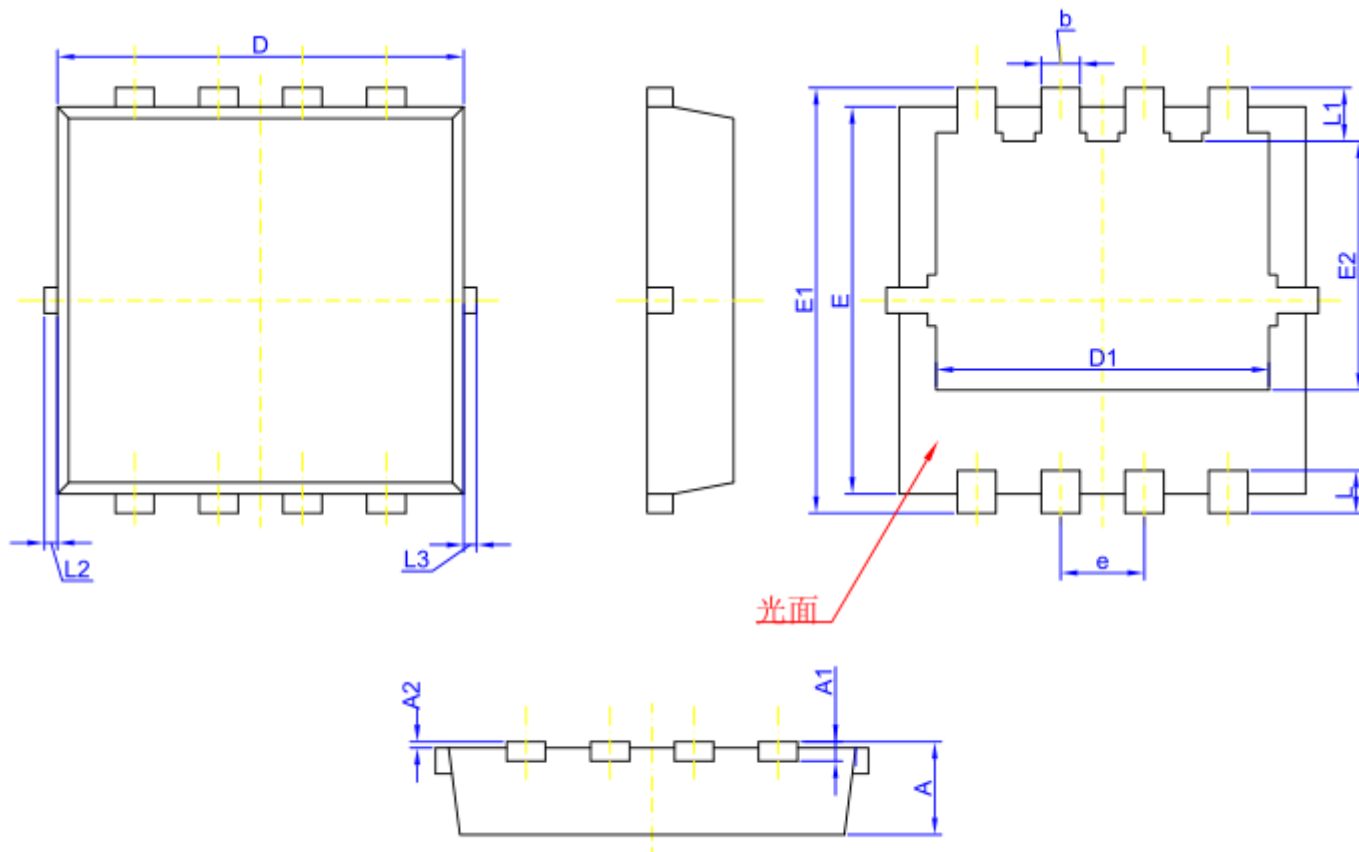
The circuit diagram on the left shows a MOSFET (DUT) switching an inductive load (RL) from a supply (VDD). The gate is driven by a voltage source (VGS) through a resistor (RG). The drain is connected to the load and the supply. The load voltage (VDS) is measured across the inductor. The waveforms on the right show the gate voltage (VGS) as a square wave and the drain voltage (VDS) as a trapezoidal wave. The 90% and 10% voltage levels are marked on the VDS waveform to define the switching times: t_{on} (turn-on time) and t_{off} (turn-off time). The trapezoidal shape of the VDS waveform during switching is characteristic of an inductive load.

The circuit diagram shows a MOSFET (DUT) with gate resistor R_g and drain inductor L . The gate voltage V_{gs} is a square wave. The drain voltage V_{ds} and drain current I_d waveforms are shown, illustrating the switching transient. The formula $E_{AR} = 1/2 L I_{AR}^2$ is provided.

Figure 1: Schematic diagram and waveforms for the turn-off test of a MOSFET. The schematic shows a MOSFET (DUT) with a drain inductor L , driven by a gate voltage V_{gs} and a drain voltage V_{ds} . A current source I_{dt} is connected to the drain. The waveforms show V_{gs} , I_{dt} , and V_{ds} over time. The turn-off time t_{rr} is defined as the time from the start of the drain current I_{dt} to the point where the drain voltage V_{ds} reaches its peak value V_{dd} .

8. Package Dimensions

PDFN3.3*3.3 Package



Symbol	Dimensions In Millimeters		
	MIN.	NOM.	MAX.
A	0.700	0.800	0.900
A1	0.100	0.150	0.200
A2	-	-	0.050
D	3.000	3.100	3.200
D1	2.350	2.450	2.550
E	3.000	3.100	3.200
E1	3.200	3.400	3.600
E2	1.635	1.735	1.835
b	0.200	0.300	0.400
e	0.550	0.650	0.750
L	0.250	0.450	0.650
L1	0.345	0.545	0.745
L2	0~0.100		
L3	0~0.100		

9. Record of Document amendment

产品名称: LN490N150Q

文档类型: 产品手册

版权说明: 镭诺电子(宁波)有限公司

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公司主页: www.leinuosemi.com

版本: 01

修改记录:

1.初版发行