

100V N-Channel Enhancement Mode MOSFET

1.Product Information

1.1 Features

- ◇ Advanced SGT cell design
- ◇ Low Gate Charge
- ◇ Low On-Resistance
- ◇ RoHS and Halogen-Free Compliant
- ◇ 100% ΔV_{DS} & UIS & Rg Tested

1.2 Applications

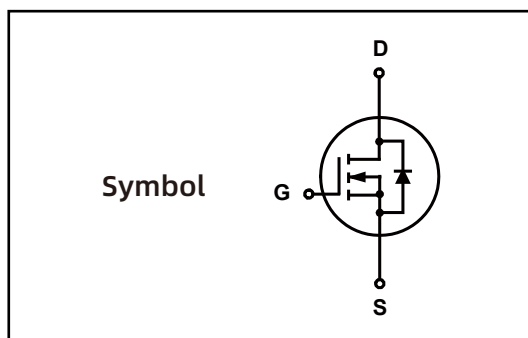
- ◇ DC-DC Converter
- ◇ Drones
- ◇ Motor drivers
- ◇ Light electric vehicles

1.3 Quick reference

- ◇ $BV \geq 100\text{ V}$
- ◇ $P_{\text{tot}} \leq 328\text{ W}$
- ◇ $I_D \leq 325\text{ A}$
- ◇ $R_{DS(ON)} \leq 2.4\text{ m}\Omega @ V_{GS} = 10\text{V}$
- ◇ $R_{DS(ON)} \leq 3.5\text{ m}\Omega @ V_{GS} = 6.0\text{V}$

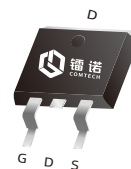


2.Pin Description



Simplified Outline

Top View
TO-263-3L



3.Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit	Note
V_{DS}	Drain-Source Voltage	$T_C = 25\text{ }^{\circ}\text{C}$	-	100	V	-
V_{GS}	Gate-Source Voltage	$T_C = 25\text{ }^{\circ}\text{C}$	-	± 20	V	-
I_D^*	Drain Current (DC)	$T_C = 25\text{ }^{\circ}\text{C}, V_{GS} = 10\text{ V}$	-	325	A	Fig.2
		$T_C = 100\text{ }^{\circ}\text{C}, V_{GS} = 10\text{ V}$	-	205	A	
$I_{DM}^{**},^{***}$	Drain Current (Pulsed)	$T_C = 25\text{ }^{\circ}\text{C}, V_{GS} = 10\text{ V}$	-	571	A	-
P_{tot}	Drain power dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	-	328	W	Fig.1
		$T_C = 100\text{ }^{\circ}\text{C}$	-	131	W	
	Linear reduction	$T_A > 25\text{ }^{\circ}\text{C}$	-	2.63	W/ $^{\circ}\text{C}$	
T_{stg}	Storage Temperature		-55	150	$^{\circ}\text{C}$	-
T_J	Junction Temperature		-	150	$^{\circ}\text{C}$	-
I_S	Continuous-Source Current	$T_C = 25\text{ }^{\circ}\text{C}$	-	325	A	-
E_{AS}^*	Single Pulsed Avalanche Energy	$V_{DD} = 100\text{ V}, L = 0.5\text{ mH}$	-	1239	mJ	Fig.19

4.Thermal Characteristics

$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient	-	13	$^{\circ}\text{C/W}$	Fig.16
$R_{\theta JC}^*$	Thermal Resistance- Junction to Case	-	0.38		

Notes :

- * Surface Mounted on 1 in² pad area, $t \leq 10\text{ sec}$
- ** Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- *** limited by bonding wire

5.Marking Information

Product Name	Package	Reel size	Tape width	Quantity	Note
LN014N100K	TO-263-3L	330mm	24mm	800	

Note: COMTECH defines “ Green ” as lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C)

6. Electrical Characteristics ($T_A=25^\circ$ Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
Static Characteristics							
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _{DS} = 250 μA	100	-	-	V	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	2	-	4	V	
I _{DSS}	Drain Leakage Current	V _{DS} =100V, V _{GS} = 0 V	-	-	1	μA	
I _{GSS}	Gate Leakage Current	V _{GS} = ± 20 V, V _{DS} = 0 V	-	-	±100	nA	
R _{DS(ON)} ^a	On-State Resistance	V _{GS} =10V , I _{DS} =20A	-	2.2	2.4	mΩ	Fig.8
		V _{GS} =6.0V, I _{DS} =10A	-	3.0	3.5		
Diode Characteristics							
V _{SD} ^a	Diode Forward Voltage	I _{SD} = 20A, V _{GS} = 0 V	-	-	1.3	V	Fig.7
t _{rr}	Reverse Recovery Time	I _{DS} = 20A, V _{GS} = 0 V dI _{SD} /dt = 100 A/μs	-	66	-	nS	Fig.20
Q _{rr}	Reverse Recovery Charge		-	135	-	nC	
Dynamic Characteristics ^b							
C _{ISS}	Input Capacitance	V _{GS} = 0 V, V _{DS} =50V Frequency = 1 MHz	-	6643	-	pF	Fig.10
C _{OSS}	Output Capacitance		-	2848	-		
C _{rSS}	Reverse Transfer Capacitance		-	92	-		
R _G	Gate Resistance	F= 1 MHz	-	0.4	-	Ω	
t _{d(on)}	Turn-on Delay Time	V _{DS} =50V , V _{GS} = 10 V, RG _(ext) =2.7Ω , RL =20uH I _{DS} =20A	-	38	-	nS	Fig.18
t _r	Turn-on Rise Time		-	85	-		
t _{d(off)}	Turn-off Delay Time		-	62	-		
t _f	Turn-off Fall Time		-	25	-		
dv/dt(on)	Turn-on Peak Diode Recovery		-	0.469	-	KV/us	
dv/dt(off)	Turn-off Peak Diode Recovery		-	1.592	-		
di/dt(on)	Turn-on Peak Diode Recovery		-	561	-	A/us	
di/dt(off)	Turn-off Peak Diode Recovery		-	497	-		
Gate Charge Characteristics ^b							
Q _g	Total Gate Charge	V _{DS} =50V , V _{GS} = 10 V, I _{DS} = 20A	-	100	-	nC	Fig.9
Q _{gs}	Gate-Source Charge		-	23	-		
Q _{gd}	Gate-Drain Charge		-	41	-		
V _{plateau}	Gate plateau voltage		-	4.4	-	V	

Notes :

a : Pulse test ; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b : Guaranteed by design, not subject to production testing

7. Typical Characteristics

Fig.1 Power Capability

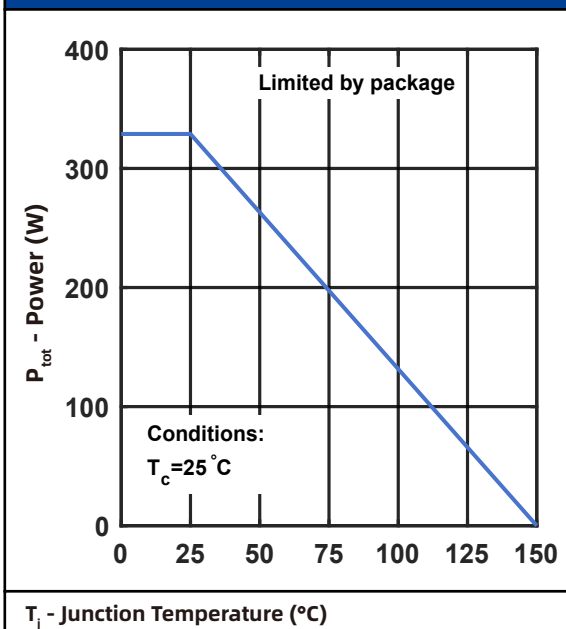


Fig.2 Current Capability

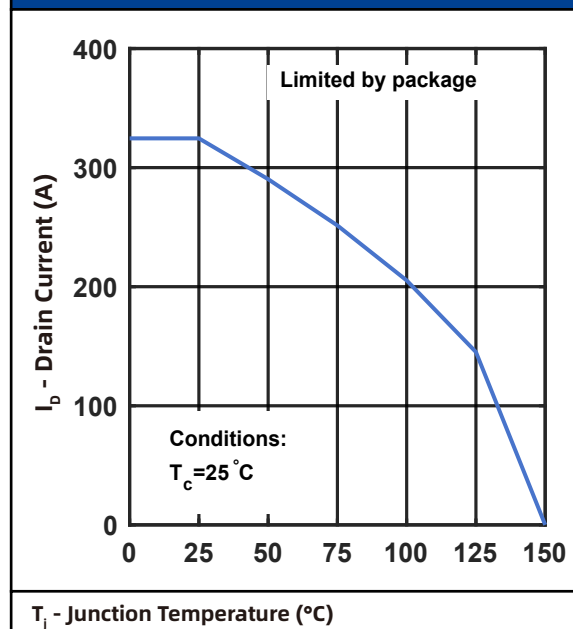


Fig.3 Output Characteristics@ $T_j = -55^\circ\text{C}$

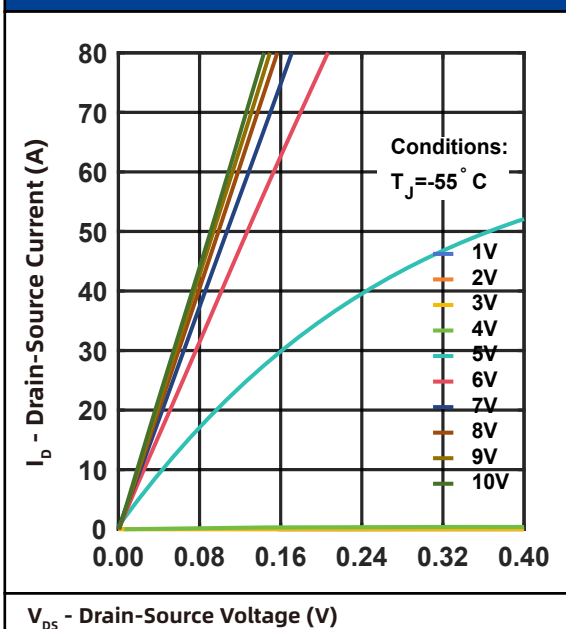
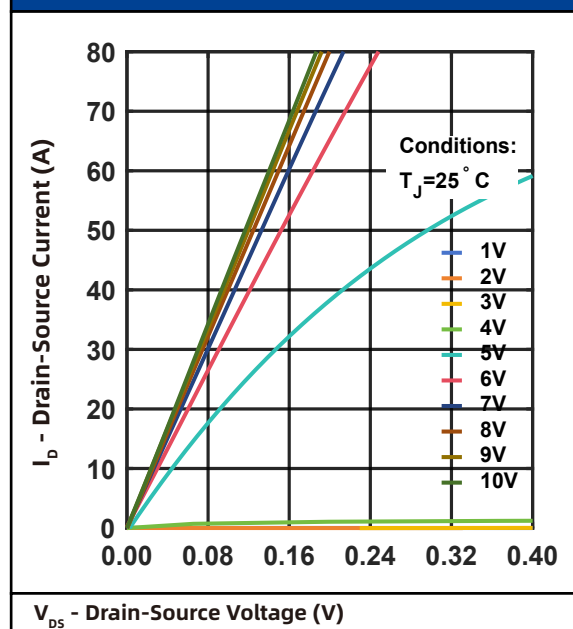


Fig.4 Output Characteristics@ $T_j = 25^\circ\text{C}$



7. Typical Characteristics

Fig.5 Output Characteristics@Tj 150°C

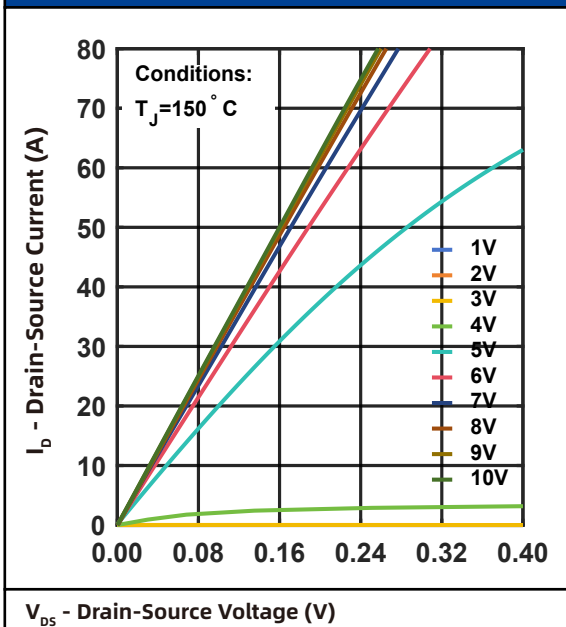


Fig.6 Transfer Characteristics vs Temp

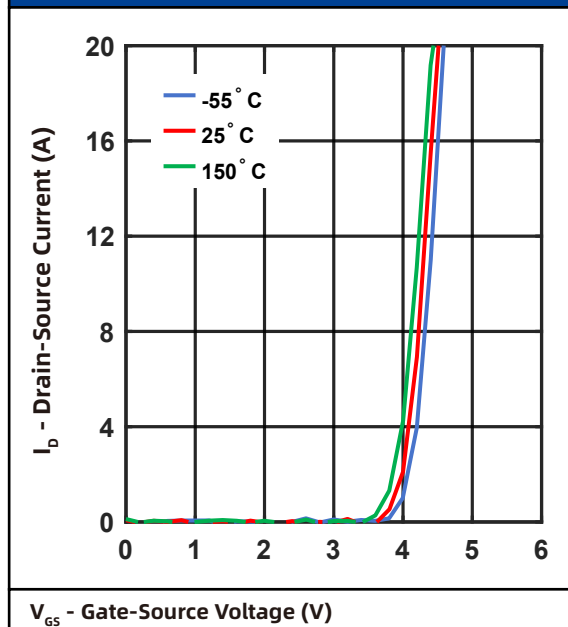


Fig.7 Body Diode Characteristics

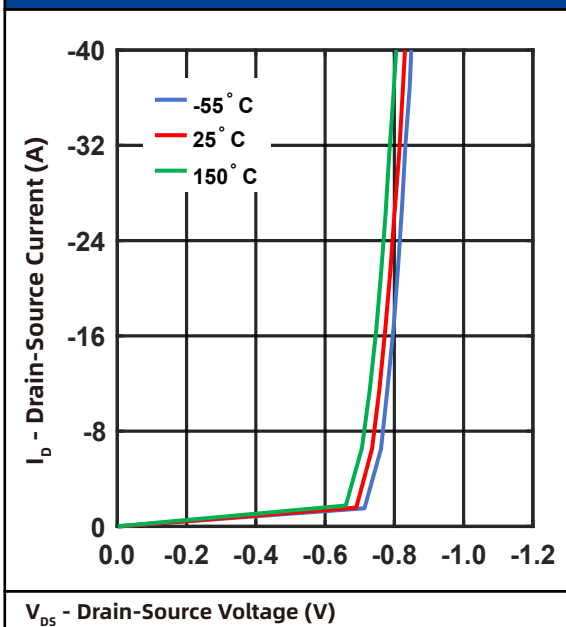
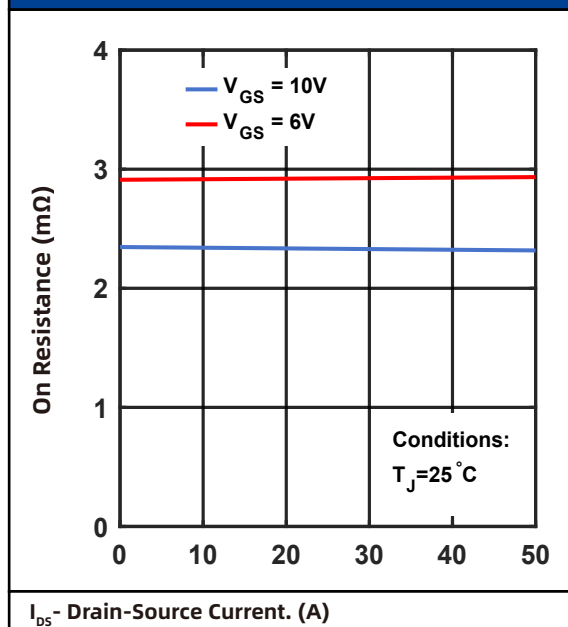
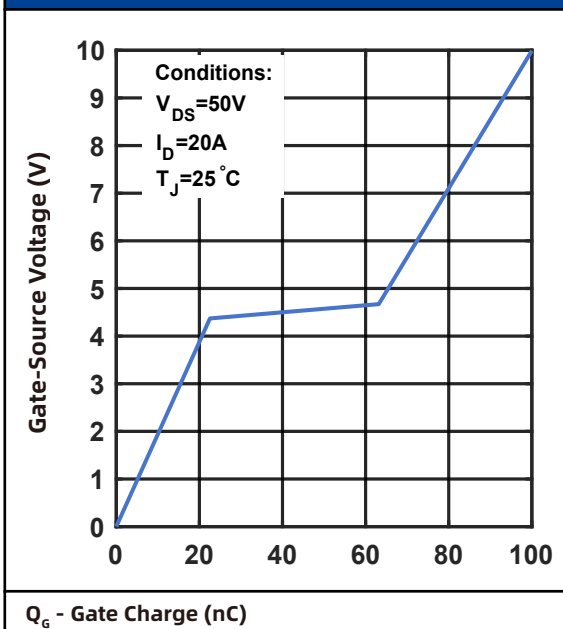
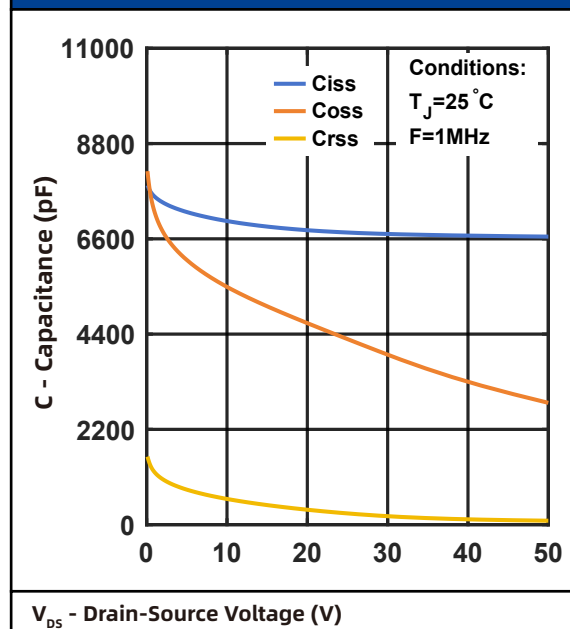
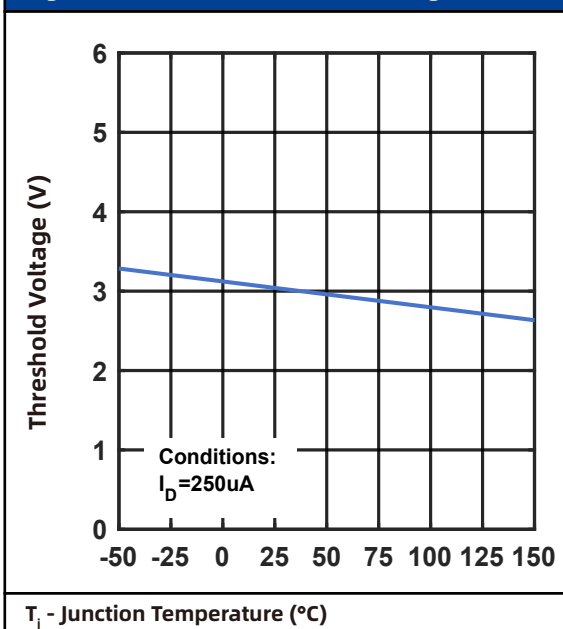
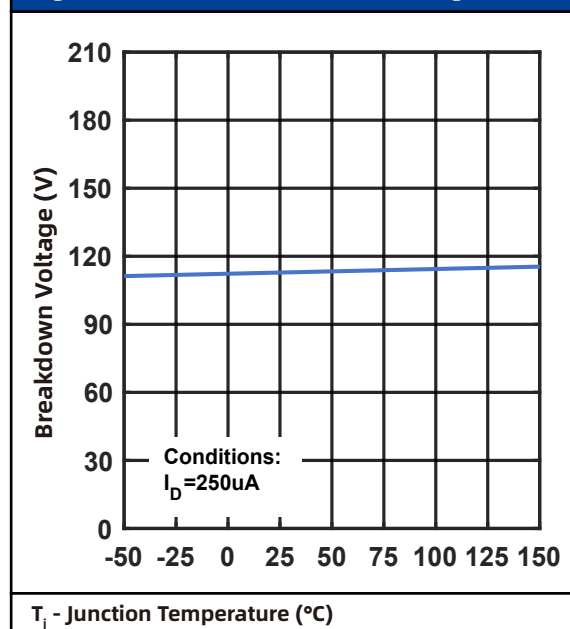


Fig.8 Drain-Source On Resistance



7. Typical Characteristics

Fig.9 Gate Charge

Fig.10 Capacitance

Fig.11 Normalized Threshold Voltage

Fig.12 Normalized Breakdown Voltage


7. Typical Characteristics

Fig.13 Normalized On Resistance

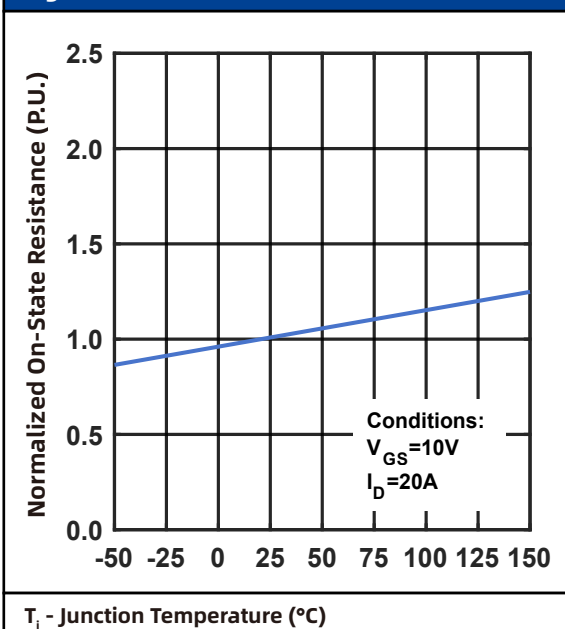


Fig.14 Switching Energy vs ID

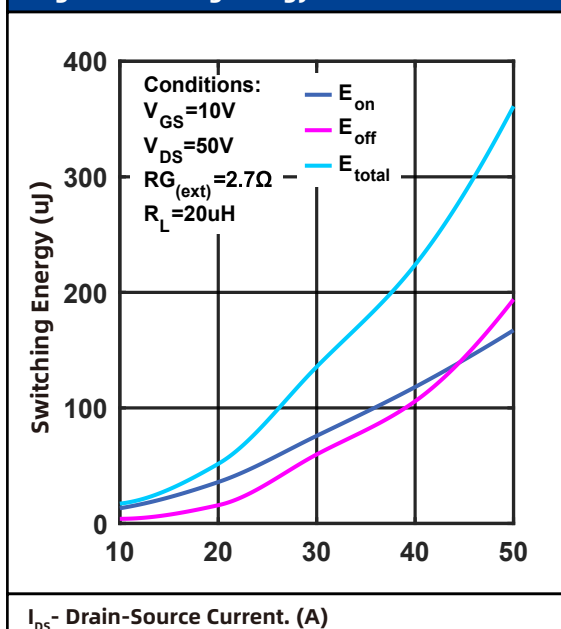


Fig.15 Safe Operating Area

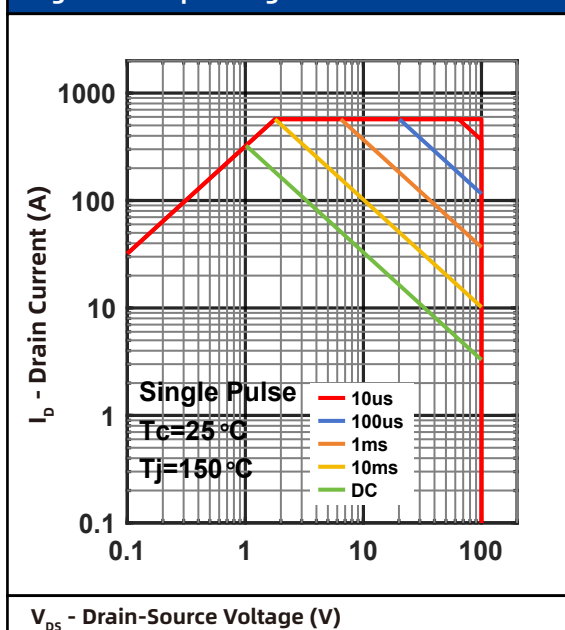
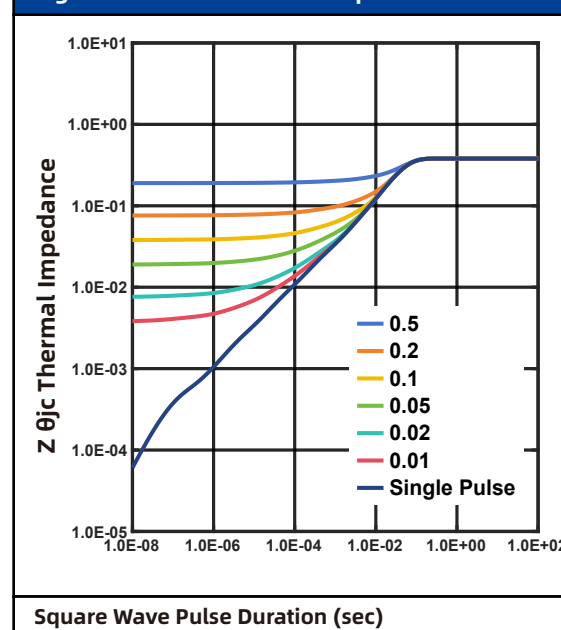


Fig.16 Transient Thermal Impedance



7. Typical Characteristics

Fig.17 Gate Charge Test Circuit & Waveform

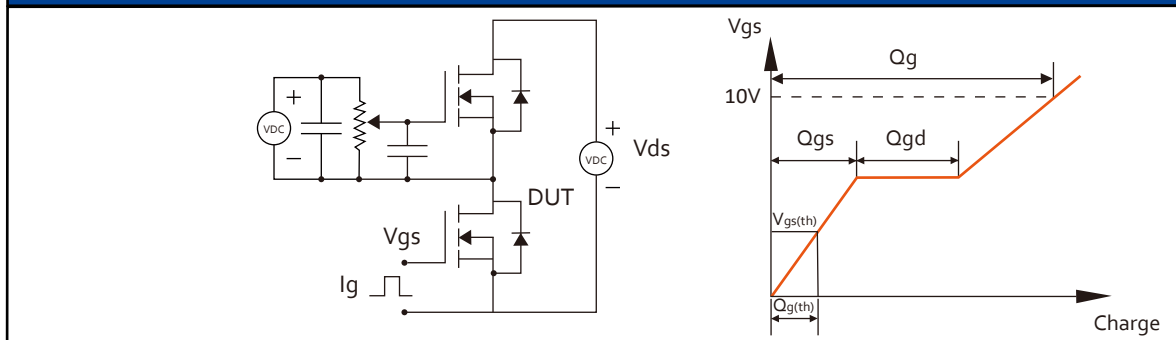


Fig.18 Resistive Switching Test Circuit & Waveforms

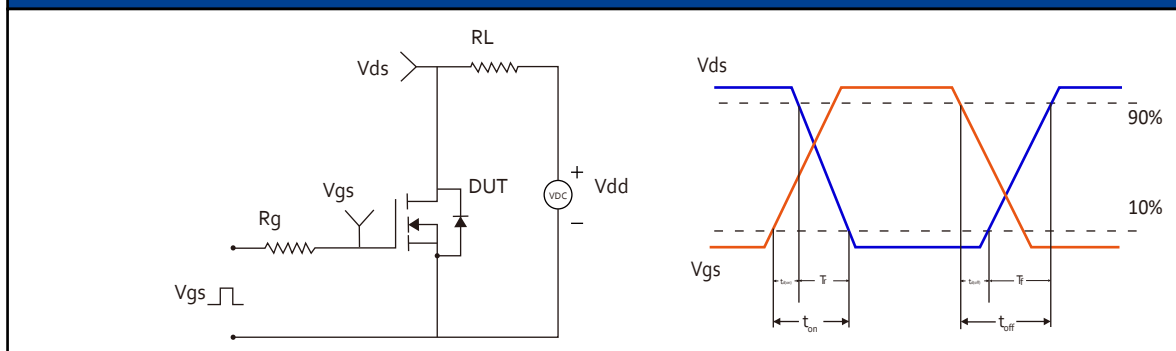


Fig.19 Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

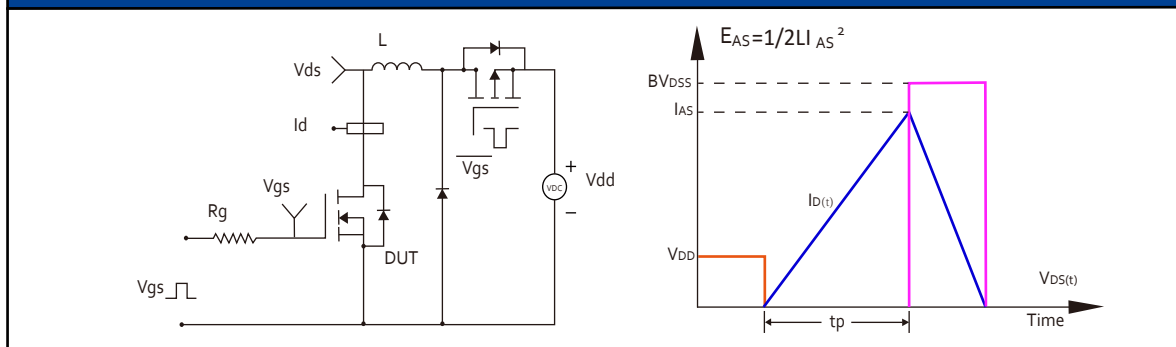
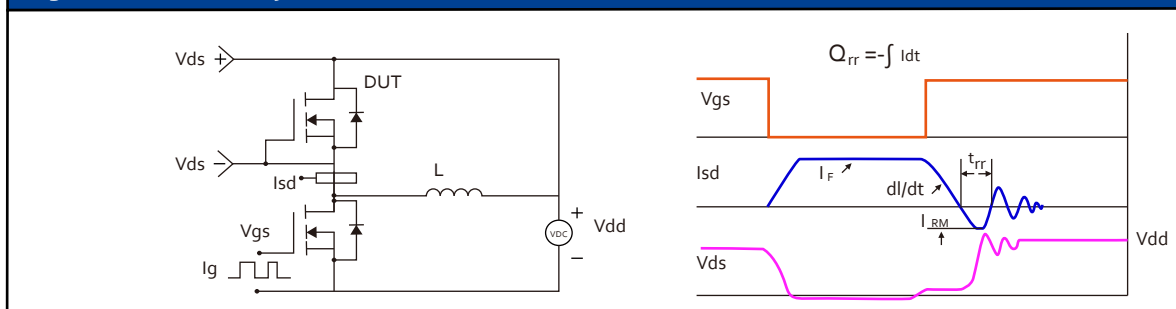
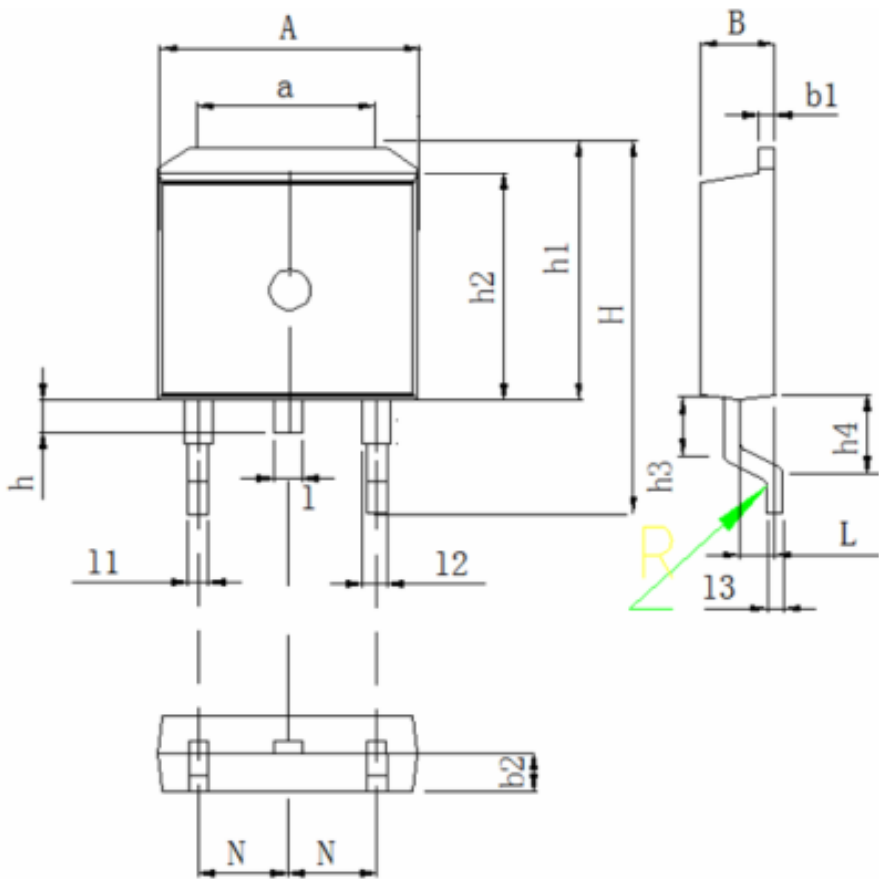


Fig.20 Diode Recovery Test Circuit & Waveforms



8. Package Dimensions

TO-263-3L Package



Symbol	Dimensions In Millimeters		
	MIN.	NOM.	MAX.
A	9.60	9.80	10.00
a	7.20	7.40	7.60
B	4.30	4.50	4.70
b1	1.25	1.30	1.35
b2	2.20	2.40	2.60
H	15.20	15.50	15.80
h	1.34	1.54	1.74
h1	10.30	10.50	10.70
h2	9.10	9.20	9.30
h3	1.34	1.54	1.74
h4	2.50	2.70	2.90
L	2.20	2.40	2.60
l	1.20	1.30	1.40
l1	0.70	0.80	0.90
l2	1.20	1.30	1.40
l3	0.40	0.50	0.60
N	2.40	2.45	2.50
R	0.45R	0.50R	0.55R



9. Record of Document amendment

产品名称: LN014N100K

文档类型: 产品手册

版权说明: 镭诺电子(宁波)有限公司

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公司主页: www.leinuosemi.com

版本: 01

修改记录:

1.初版发行