

## 40V N-Channel Enhancement Mode MOSFET

### 1. Product Information

#### 1.1 Features

- ◇ Advanced SGT cell design
- ◇ Low Gate Charge
- ◇ Low On-Resistance
- ◇ RoHS and Halogen-Free Compliant
- ◇ 100%  $\Delta V_{DS}$  & UIS & Rg Tested

#### 1.2 Applications

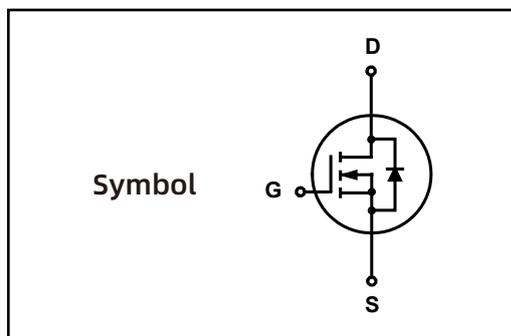
- ◇ DC-DC Converter
- ◇ Drones
- ◇ Motor drivers
- ◇ Light electric vehicles

#### 1.3 Quick reference

- ◇  $BV \cong 40\text{ V}$
- ◇  $P_{\text{tot}} \cong 62\text{ W}$
- ◇  $I_D \cong 135\text{ A}$
- ◇  $R_{DS(\text{ON})} \cong 2.5\text{ m}\Omega @ V_{GS} = 10\text{ V}$
- ◇  $R_{DS(\text{ON})} \cong 5\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$



### 2. Pin Description



### 3.Limiting Values

Symbol	Parameter	Conditions	Min	Max	Unit	Note
$V_{DS}$	Drain-Source Voltage	$T_C = 25\text{ }^\circ\text{C}$	-	40	V	-
$V_{GS}$	Gate-Source Voltage	$T_C = 25\text{ }^\circ\text{C}$	-	$\pm 20$	V	-
$I_D^*$	Drain Current ( DC )	$T_C = 25\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	135	A	Fig.2
		$T_C = 100\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	85	A	
$I_{DM}^{**},^{***}$	Drain Current ( Pulsed )	$T_C = 25\text{ }^\circ\text{C}, V_{GS} = 10\text{ V}$	-	324	A	-
$P_{tot}$	Drain power dissipation	$T_C = 25\text{ }^\circ\text{C}$	-	62	W	Fig.1
$T_{stg}$	Storage Temperature		-55	150	$^\circ\text{C}$	-
$T_J$	Junction Temperature		-	150	$^\circ\text{C}$	-
$I_S$	Continuous-Source Current	$T_C = 25\text{ }^\circ\text{C}$	-	135	A	-
$E_{AS}^*$	Single Pulsed Avalanche Energy	$V_{DD} = 40\text{ V}, L = 10\text{ }\mu\text{H}$	-	90	mJ	Fig.19

### 4.Thermal Characteristics

$R_{\theta JA}^*$	Thermal Resistance- Junction to Ambient	-	42	$^\circ\text{C}/\text{W}$	Fig.16
$R_{\theta JC}^*$	Thermal Resistance- Junction to Case	-	2		

Notes :

\* Surface Mounted on 1 in<sup>2</sup> pad area,  $t \leq 10\text{ sec}$

\*\* Pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$

\*\*\* limited by bonding wire

### 5.Marking Information

Product Name	Package	Reel size	Tape width	Quantity	Note
LN020N040J	T0252	330mm	12mm	2500	

Note: COMTECH defines " Green " as lead-free ( RoHS compliant ) and halogen free ( Br or Cl does not exceed 900 ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500 ppm by weight; Follow IEC 61249-2-21 and IPC / JEDEC J-STD-020C )

## 6. Electrical Characteristics ( $T_A=25^\circ$ Unless Otherwise Noted )

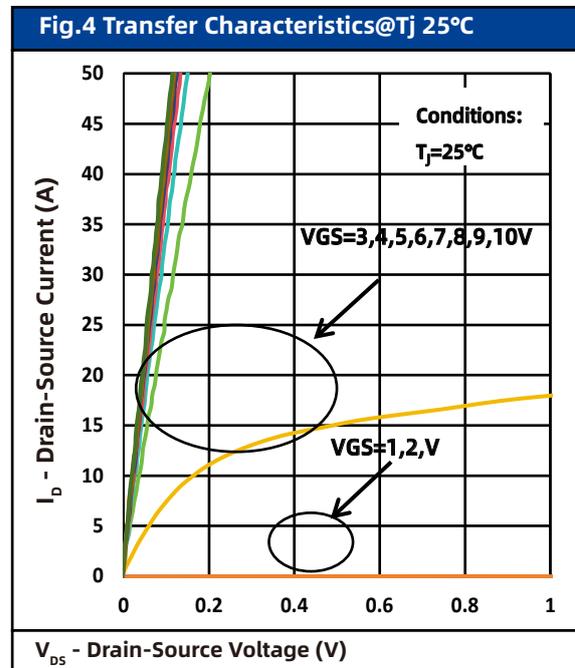
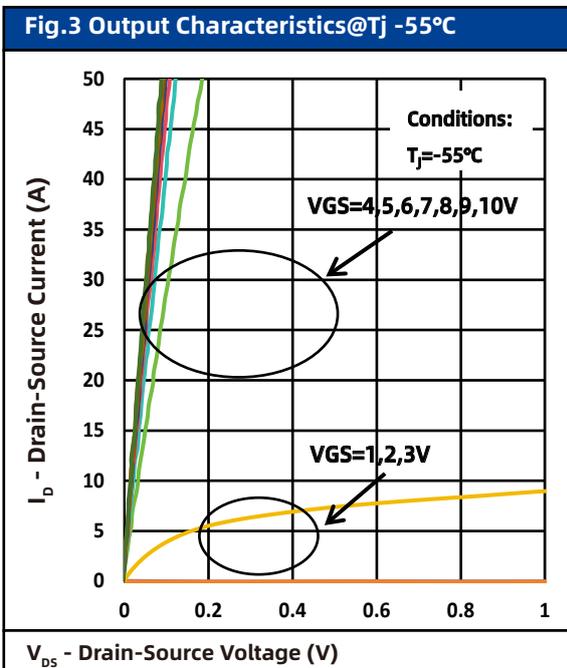
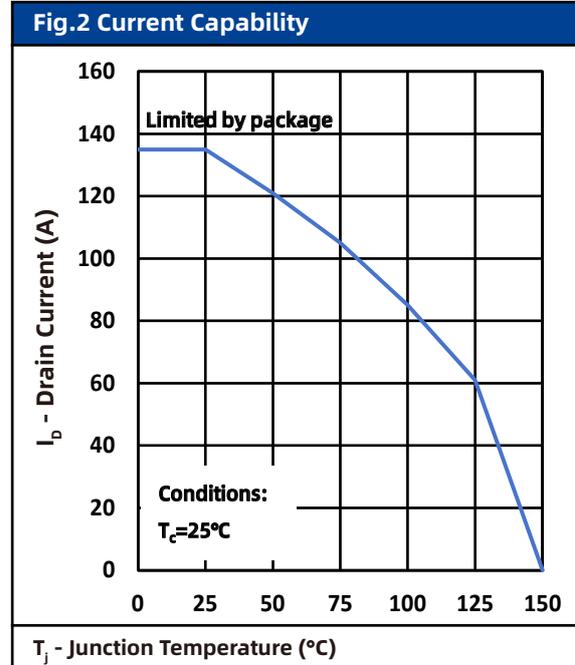
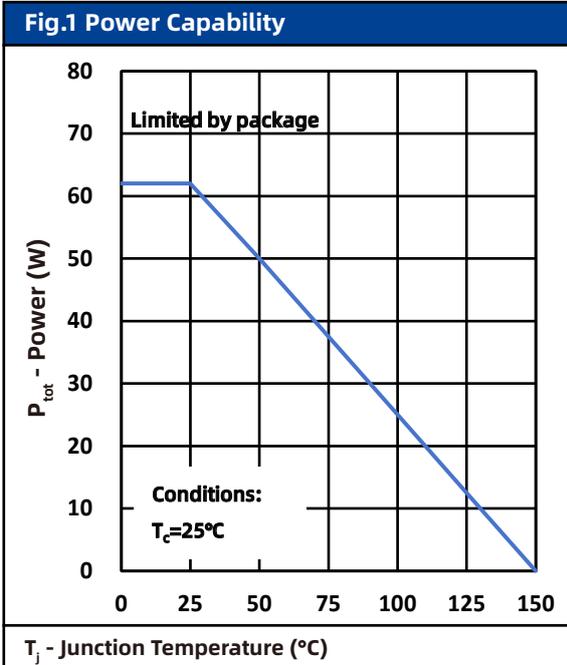
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
<b>Static Characteristics</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	40	-	-	V	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	1	-	3	V	
$I_{DSS}$	Drain Leakage Current	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$	
$I_{GSS}$	Gate Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA	
$R_{DS(on)}^a$	On-State Resistance	$V_{GS} = 10\text{ V}, I_{DS} = 50\text{ A}$	-	2.3	2.5	m $\Omega$	Fig.8
		$V_{GS} = 4.5\text{ V}, I_{DS} = 20\text{ A}$	-	3.2	3.5		
<b>Diode Characteristics</b>							
$V_{SD}^a$	Diode Forward Voltage	$I_{DS} = 20\text{ A}, V_{GS} = 0\text{ V}$	-	-	1.3	V	Fig.7
$t_{rr}$	Reverse Recovery Time	$I_{DS} = 50\text{ A}, V_{GS} = 0\text{ V}$	-	33	-	nS	Fig.20
$Q_{rr}$	Reverse Recovery Charge	$dI_{SD}/dt = 100\text{ A}/\mu\text{s}$	-	44	-	nC	
<b>Dynamic Characteristics<sup>b</sup></b>							
$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$ Frequency = 1 MHz	-	3050	-	pF	Fig.10
$C_{OSS}$	Output Capacitance		-	530	-		
$C_{rSS}$	Reverse Transfer Capacitance		-	500	-		
$R_G$	Gate Resistance	F= 1 MHz	-	1.9	-	$\Omega$	
$t_d(on)$	Turn-on Delay Time	$V_{DS} = 20\text{ V}, V_{GEN} = 10\text{ V},$ $R_G=2.8\ \Omega, R_L = 10\ \mu\text{H},$ $I_{DS} = 20\text{ A}$	-	13	-	nS	Fig.18
$t_r$	Turn-on Rise Time		-	205	-		
$t_d(off)$	Turn-off Delay Time		-	41	-		
$t_f$	Turn-off Fall Time		-	27	-		
$dv/dt$	Peak Diode Recovery		-	0.078	-		
$di/dt$	Peak Diode Recovery	-	292	-	A/us		
<b>Gate Charge Characteristics<sup>b</sup></b>							
$Q_g$	Total Gate Charge	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V},$ $I_{DS} = 20\text{ A}$	-	74	-	nC	Fig.17
$Q_{gs}$	Gate-Source Charge		-	8	-		
$Q_{gd}$	Gate-Drain Charge		-	30	-		
$V_{plateau}$	Gate plateau voltage		-	3	-		

Notes :

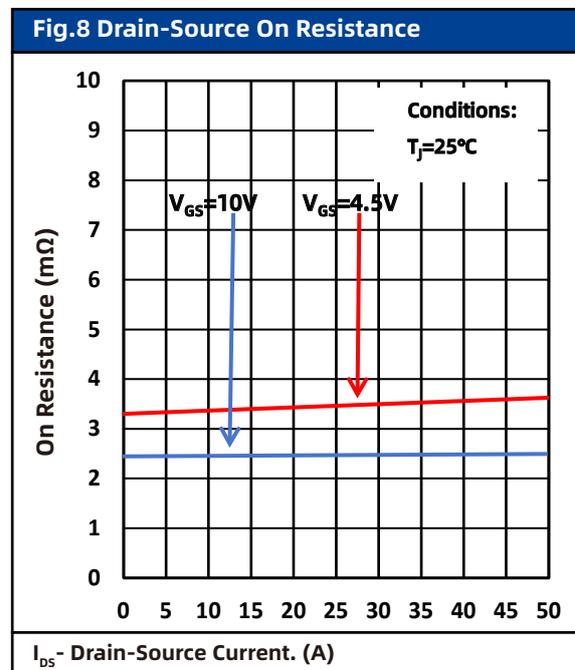
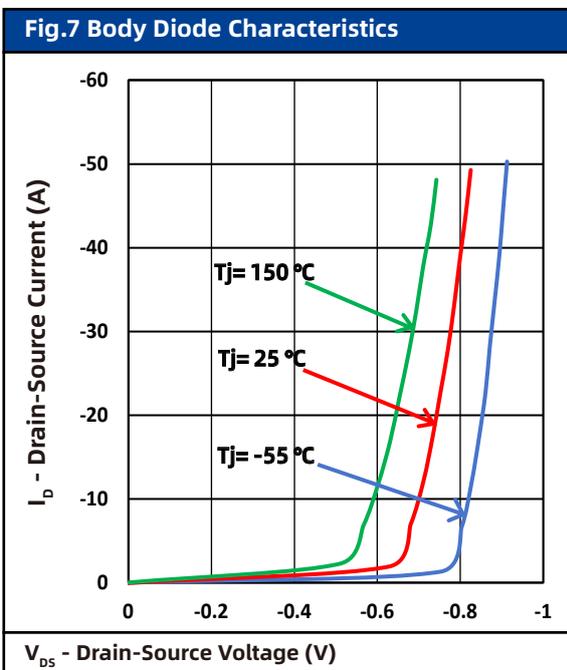
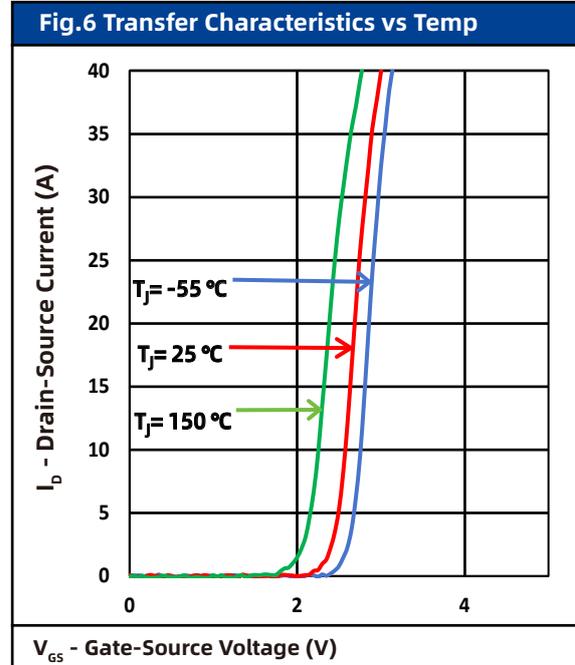
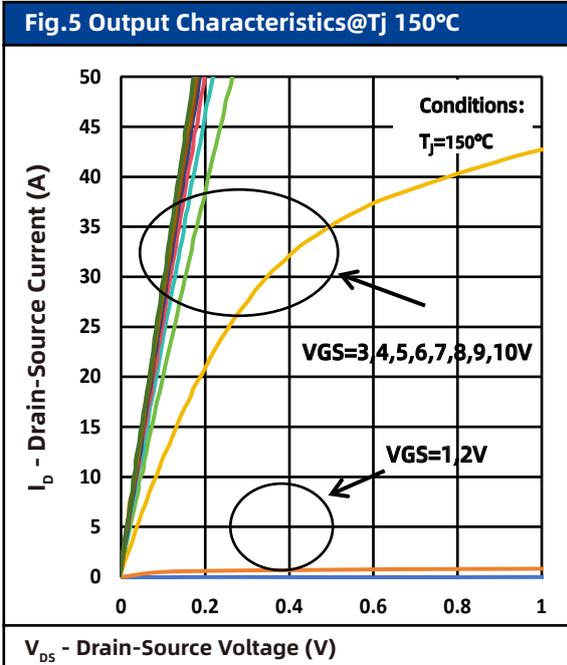
a : Pulse test ; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ 

b : Guaranteed by design, not subject to production testing

## 7. Typical Characteristics



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Fig.9 Gate Charge

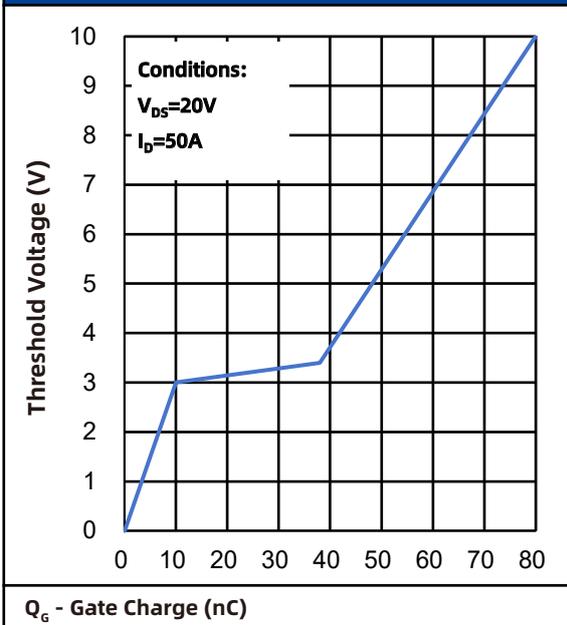


Fig.10 Capacitance

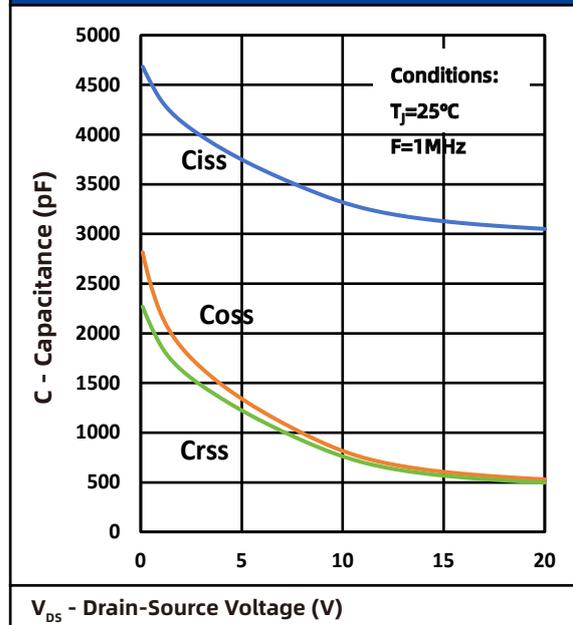


Fig.11 Normalized Threshold Voltage

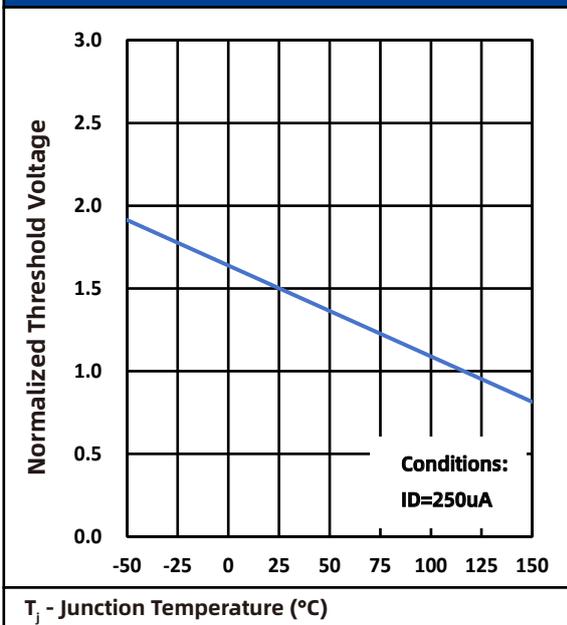
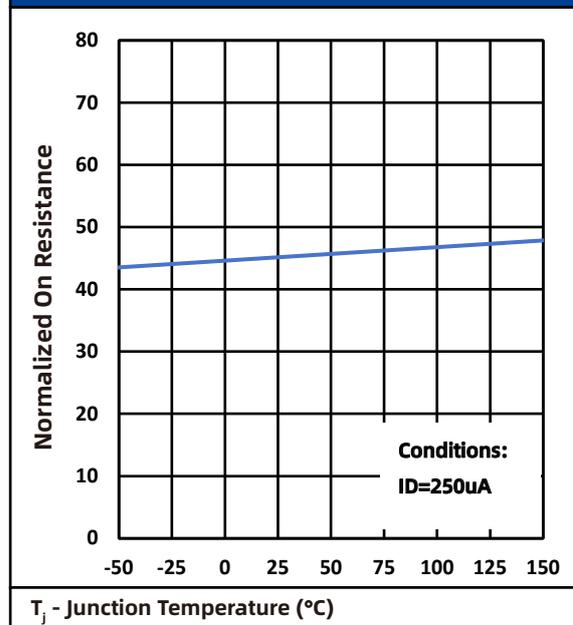


Fig.12 Normalized On Resistance



## 7. Typical Characteristics

Fig.13 Normalized On Resistance

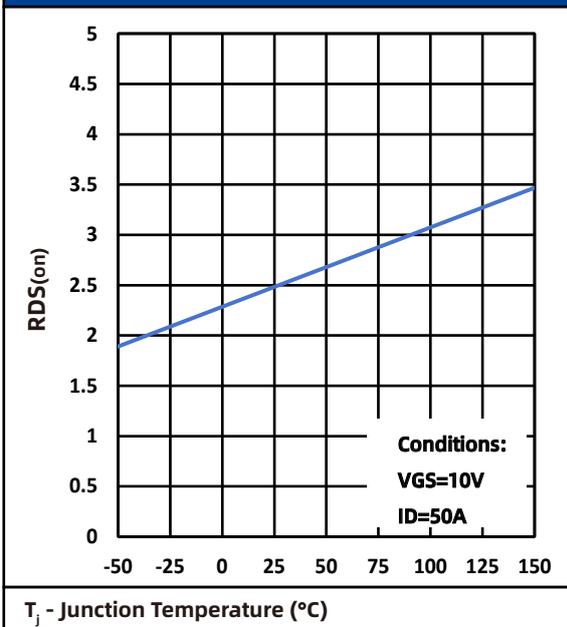


Fig.14 Switching Energy vs ID

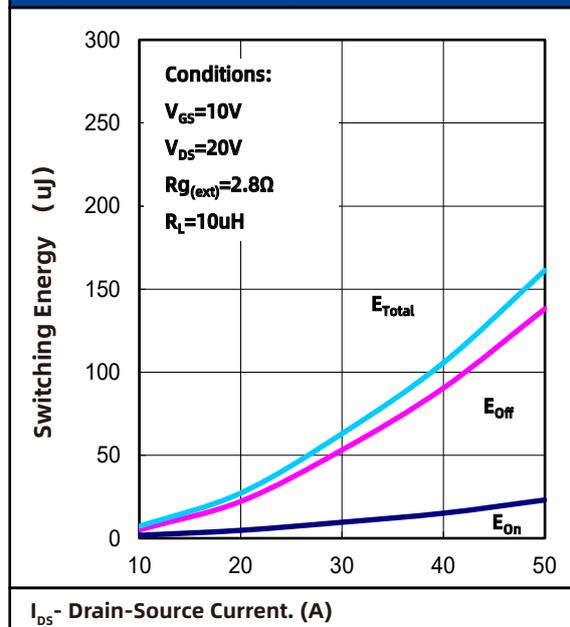


Fig.15 Safe Operating Area

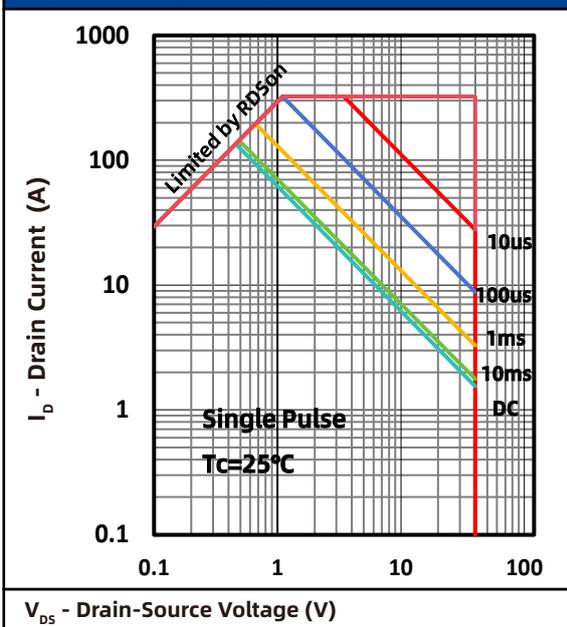
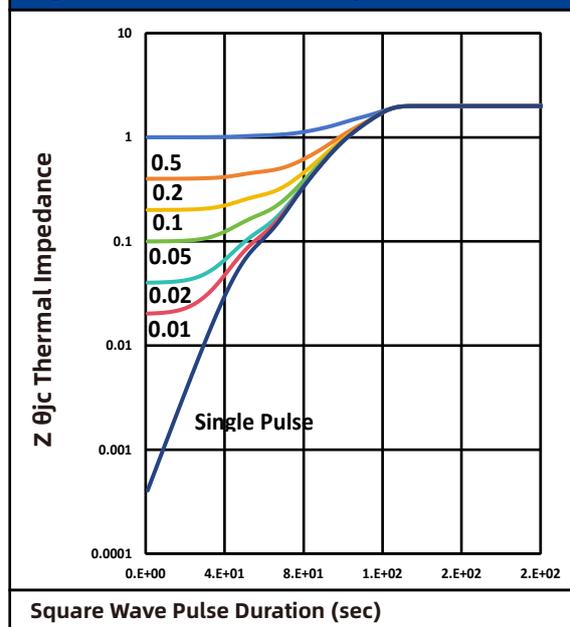


Fig.16 Transient Thermal Impedance



## 7. Typical Characteristics

Fig.17 Gate Charge Test Circuit & Waveform

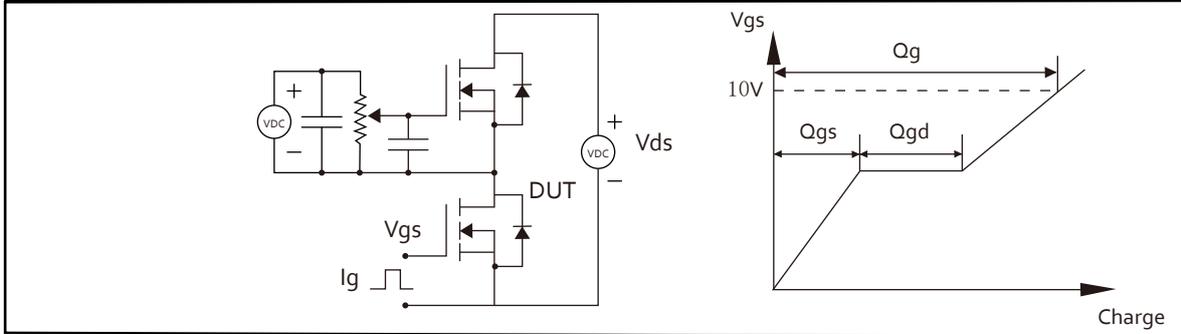


Fig.18 Resistive Switching Test Circuit & Waveforms

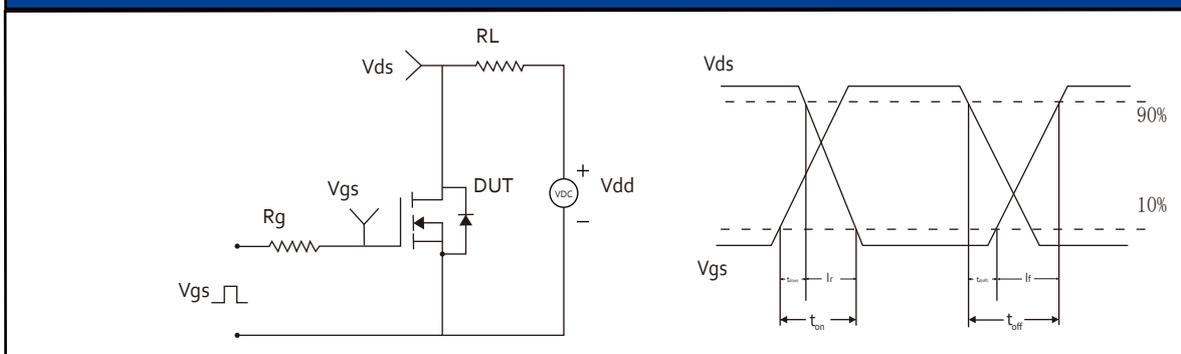


Fig.19 Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

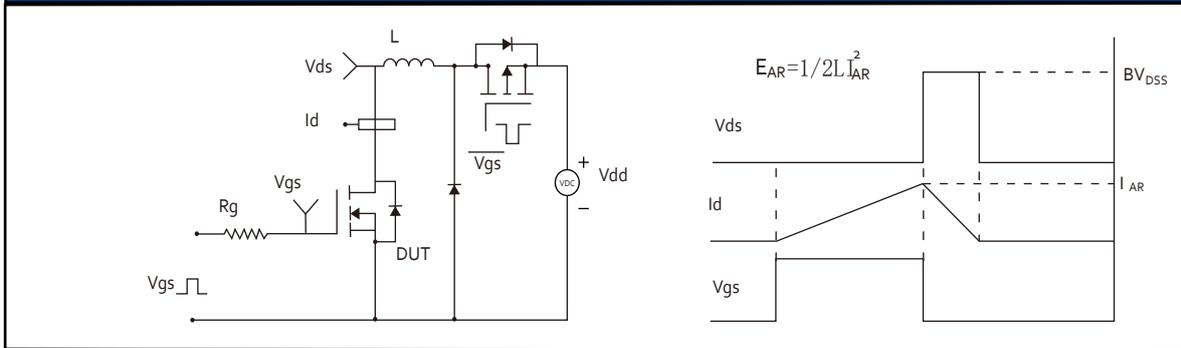
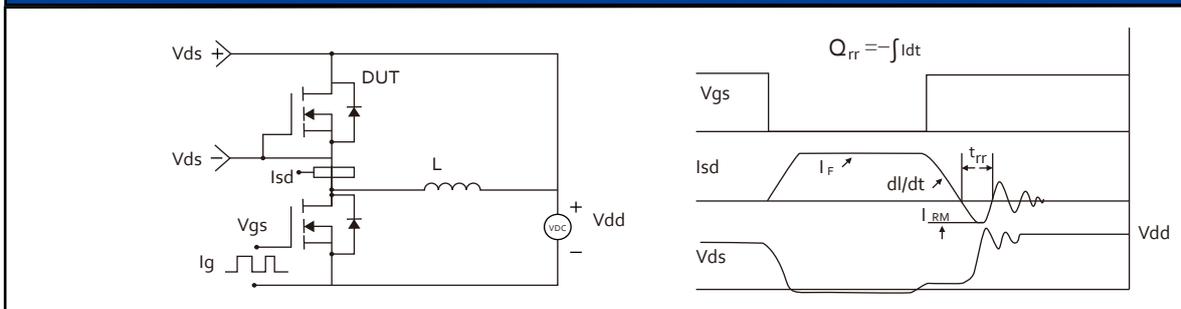
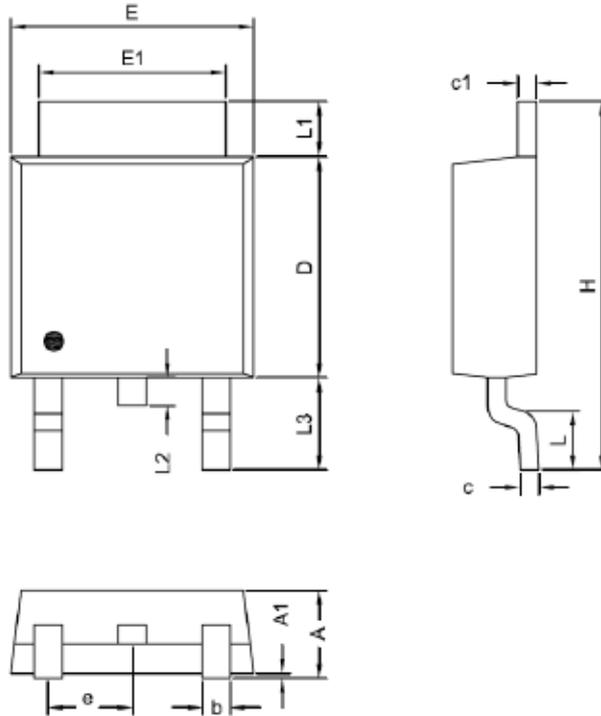


Fig.20 Diode Recovery Test Circuit & Waveforms



## 8. Package Dimensions

### T0252 Package



Symbol	Unit : mm		Unit : inch	
	MIN	MAX	MIN	MAX
A	2.080	2.500	0.082	0.098
A1	0.000	0.250	0.000	0.010
D	5.300	6.400	0.209	0.252
E	6.100	6.850	0.240	0.270
E1	4.676	5.650	0.184	0.222
c	0.400	0.650	0.016	0.026
c1	0.400	0.650	0.016	0.026
b	0.500	1.000	0.020	0.039
e	2.090	2.500	0.082	0.098
L	1.000	1.800	0.039	0.071
L1	0.700	1.800	0.028	0.071
L2	0.500	1.200	0.020	0.047
L3	2.400	3.070	0.094	0.121
H	9.000	10.700	0.354	0.421

## 9. Record of Document amendment

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1.初版发行